Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, NOV/DEC 2024

ELECTRONICS AND COMMUNICATION ENGINEERING

SEMESTER VI

EC5651 DIGITAL VLSI

(Regulation2019)

Time:3hrs

Max. Marks: 100

CO1	Ability to analyze MOS devices and inverter
CO2	Ability to design and analyze Combinational logic
CO3	Ability to design and analyze Sequential logic
CO4	Ability to design and analyze Data path cells
CO5	Ability to design Digital logic using FPGA

BL – Bloom's Taxonomy Levels

(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)

(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
1	Write the expression for the logical effort and parasitic delay of an input NOR gate.	2	CO1	L2
2	What is Channel – length modulation.	2	CO1	L1
3	What are the methods to reduce dynamic power dissipation?	2	CO2	L2
4	Draw XOR gate and XNOR gate using transmission gate.	2	CO2	L3
5	What do you mean by Set up time and Hold time?	2	CO3	L2
6	Differentiate between clock skew and clock jitter.	2	CO3	L2
7	Define booth encoding write the expression.	2	CO4	L1
8	Give the applications of high speed adder.	2	CO4	L1
9	Write the various ways of routing procedure.	2	CO5	L3
10	List the advantages of CBIC.	2	CO5	L1

PART- B (5x 13=65Marks)

Q.No.	Questions	Marks	CO	BL
11 (a)	(i) Define the need of scaling and describe the fundamental units of CMOS inverter.	5	CO1	L3
	(ii) Write the Layout design rules and draw the layout diagram for NAND and NOR gate.	8	CO1	L3
	OR			
11 (b)	Draw and explain the DC and Transfer characteristics of CMOS inverter with necessary conditions for the different regions of operations.	13	CO1	L3
12 (a)	Write a short notes with neat diagram (i) Ratioed logic (ii) Domino logic	13	CO2	L2

	OR			
12 (b)	Write a brief notes on pass transistor circuits also explain about CMOS with transmission gate.	**13**	CO2	L2
13 (a)	(i) Explain the operation of Master slave based edge triggered register.	7	CO3	L3
	(ii) Explain in detail clock distribution techniques in synchronous.	**6**	CO3	L3
	OR			
13 (b)	Elaborate the Memory Architecture in detail with classifications.	**13**	CO3	L3
14 (a)	Design 16-bit carry by pass and carry select adder and discussion their features.	**13**	CO4	L2
	OR			
14 (b)	(i) Discuss the detail about speed and area trade off.	**5**	CO4	L2
	(ii) Elaborate the operation of Barrel Shifter with neat sketch.	**8**	CO4	L2
15 (a)	Explain in detail different types of ASIC with neat diagram.	**13**	CO5	L2
	OR			
15 (b)	Describe in detail about building block Architecture of FPGA, mention the applications.	**13**	CO5	L2

PART- C (1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No.	Questions	Marks	CO	BL
16.	Draw the static CMOS logic circuit for the following expression (a) Y= (A.B.C.D)' (b) Y = (D (A+BC))'	**15**	CO2	L5